REMARKS

Claims 1-10 are pending in this application. Claims 1 and 5 are independent. In light of the remarks made herein, Applicants respectfully request reconsideration and withdrawal of the outstanding rejections.

In the outstanding Official Action, the Examiner rejected claims 1 and 2 under 35 U.S.C. § 102(a and b) as being anticipated by *Thacker* (USP 5,267,235); and rejected 5 and 9-10 under 35 U.S.C. § 103(a) as being unpatentable over *Tsuboi et al.* (USP 5,140,582) in view of *Yamasaki et al.* (USP 5,539,916). Applicants respectfully traverse these rejections.

Applicants wish to thank the Examiner for indicating that claims 3-4 and 6-8 contain allowable subject matter.

Claim Rejections – 35 U.S.C. § 102

In the outstanding Official Action, the Examiner rejected claim 1 as being anticipated by *Thacker*. The Examiner asserts that *Thacker* teaches transfer control circuit B_o transferring a first pulse applied from a preceding stage (input links) to a subsequent stage (output of circuit 30) as a second pulse (output request) based on an instruction signal (not explicitly shown) enabling or disabling a transfer (col. 5, lines 24-63 request vectors in col. 6, lines 10-55).

The Examiner further asserts that *Thacker* teaches a pulse control circuit 24 receiving data transfer request pulse signal as the first pulse from the transfer control circuit 30 in the preceding stage to output a plurality of data transfer request pulse signals (request grant signals; col. 8, lines 26-64). Applicants respectfully disagree with the Examiner's characterization of this reference.

The disclosure of *Thacker* is directed to a method and apparatus for resource arbitration. The system provides a rapid one-to-one match between requesters that must arbitrate for service from one of a number of servers. Requests are presented synchronously to all servers to which access is desired. Each server selects precisely one such request and asserts a response signal so

stating to all requesters. Each requester then selects precisely one incoming grant response and re-asserts requests to all other servers. This iteration is repeated for a predetermined number of cycles, at which time substantially most of the requested matches will have been made (Abstract). For each input port, the system causes a bit pattern to be loaded into the input port buffer, which pattern represents a set of requests for access to specified ones of the output ports. In a first request phase, these requests are loaded from the associated input port buffer into the latchable request register, and are synchronously provided in parallel to every output unit in the arbitration mechanism (col. 3, lines 51-59).

Specifically, *Thacker* teaches input buffer 30 that receives cells, each of which is stored in one of N queues (col. 6, lines 10-13). Cell requests are communicated to arbitration mechanism 24. Control logic 37 for the arbitration apparatus 24 generates signals that determine when new cells are to be loaded into the queues 33 (col. 6, lines 51-58). In cooperation with the arbitration mechanism, the switching mechanism must route the cells in each input port buffer to output ports specified by the address content of each cell (col. 6, lines 65-68). The arbitration mechanism includes a coupling unit 42 which includes wires connecting each input unit 40 port to each output unit 44 of the arbitration mechanism 24 (col. 7, lines 39-41).

In contrast, the present invention set forth in claim 1 includes a transfer control circuit transferring a first pulse applied from a preceding stage to a subsequent stage as a second pulse based on an instruction signal instructing enabling or disabling a transfer; and a pulse control circuit receiving one data transfer request pulse signal **as said first pulse from said transfer control circuit in the preceding stage** to output a plurality of data transfer request pulse signals as said second pulse to the transfer control circuit in the subsequent stage.

As noted above, the Examiner is equating the transfer control circuit with input buffer 30 and the pulse control circuit as arbitration mechanism 24. As can be seen in Fig 2 and based upon the discussion noted above, arbitration mechanism 24 received signal from input buffer 30 (the transfer control circuit of the present stage), not the transfer control circuit in the preceding

stage. As such, Applicants maintain that *Thacker* fails to anticipate the present invention of claim 1. It is respectfully requested that the outstanding rejection be withdrawn.

It is respectfully submitted that claims 2 and 11 are allowable for the reasons set forth with regard to claim 1 at least based upon their dependency on claim 1.

Claim Rejections – 35 U.S.C. § 103

In support of the Examiner's rejection of claim 5, the Examiner asserts that *Tsuboi et al.* discloses a data numbering detecting means (counter 38) for detecting the number of data based on output packet information field in the data transmission path (citing to Fig. 17 and 31; col. 23, lines 40-53; col. 24, lines 6-16 for the frame number).

Claim 5 includes a data number detection means for detecting the number of data based on output packet information set to the data packet held in said data transmission path, said self-synchronous transfer control circuit outputting a transfer request pulse signal corresponding to the number of data, in response to detection of the number of data by said data number detection means. In Applicant's previous Reply, Applicants argued that although *Tsuboi et al.* teaches counting the number of packets, this teaching is insufficient to teach detecting the number of data based on output packet information set to the data packet. As recited in col. 23, lines 40-47, the counter 38 of *Tsuboi et al.* divides the packet information for every predetermined length (corresponding to the aforementioned time length). The divided packets are successively written into the received packet buffer 31. During this operation, the packet division number counter 38 counts the number of divided packet frames. However, there is no disclosure in *Tsuboi et al.* that is directed to detecting the number of data based on output packet information **set to the data packet**. The Examiner has failed to address this argument and has essentially copied his citations from the previous Official Action. Should the Examiner maintain his rejection of claim 5, Applicants respectfully request that Examiner address Applicant's arguments herein and included in the previous Reply in a new non-final Official Action.

In addition to the above arguments, Applicants respectfully submit that one of ordinary skill in the art would not be motivated to modify the teaching of *Tsuboi et al.* to operate self-synchronously. Further, if the proposed modification or combination of the prior art would change the principle of operation of the prior art invention being modified, then the teachings of the reference are not sufficient to render the claims *prima facie* obvious. *In re Ratti*, 270 F.2d 810, 123 USPQ 439 (CCPA 1959). Applicants maintain that the proposed combination of modifying *Tsuboi et al.* to operate self-synchronously would change the principle operation of the system and would, effectively, render the system inoperative for it's intended purpose. As such the Examiner's combination is wholly improper.

Tsuboi et al. fails to teach the data number detection means as set forth above, Applicants maintain that the Examiner has failed to establish *prima facie* obviousness. Further, Applicants maintain that there is no motivation to combine the teachings as asserted by the Examiner. Finally, Applicants maintain that the purported combination would change the principle operation of the system and would, effectively, render the system inoperative for it's intended purposed. For all the reasons set forth above, Applicants respectfully request that the outstanding rejection be withdrawn.

It is respectfully submitted that claim 9 is allowable for the reasons set forth above with regard to claim 5, at least based upon it's dependency on claim 5.

Conclusion

In view of the above amendment, applicant believes the pending application is in condition for allowance.

Should there be any outstanding matters that need to be resolved in the present application, the Examiner is respectfully requested to contact Catherine M. Voisinet (Reg. No. 52,327) at the telephone number of the undersigned below, to conduct an interview in an effort to expedite prosecution in connection with the present application.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 02-2448 for any additional fees required under 37 C.F.R. §§ 1.16 or 1.17; particularly, extension of time fees.

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Respectfully submitted,

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